CACHE NEWS

NEWS ABOUT COMPUTERS IN CHEMICAL ENGINEERING EDUCATION.

No. 23

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WHAT IS CACHE?

CACHE is a non-profit organization whose purpose is to promote cooperation among universities, industry, and government in the development and distribution of computer-related and/or technology-based educational aids for the chemical engineering profession.

CREATION OF THE CACHE CORPORATION

During the 1960's, the rapid growth of computer technology cha llenged educators to develop new methods of meshing the computer with the teaching of chemical engineering. In spite of many significant contributions to program development, the transferability of computer codes, even those written in FORTRAN, was minimal. Because of the disorganized state of university-developed codes for chemical engineering, 14 chemical engineering educators met in 1969 to form the CACHE (Computer Aids for Chemical Engineering) Committee. Initially, the CACHE Committee was sponsored by the Commission on Education of the National Academy of Engineering and funded by the National Science Foundation. In 1975, after several successful projects had been completed, CACHE was incorporated as a not-for-profit corporation in Massachusetts to serve as the administrative umbrella for the consortium activities.

CACHE ACTIVITIES

All CACHE activities are staffed by volunteers, including both educators and industrial members, and coordinated by the Board of Trustees through various Task Forces. CACHE actively solicits the participation of interested individuals in the work of its on-going projects. Information on CACHE activities is regularly disseminated through **CACHE NEWS**, which is published twice each year. Individual inquiries should be addressed to:

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CACHE TRUSTEES

CACHE NEWS

The **CACHE News** is published two times a year to report news of CACHE activities and other noteworthy developments of interest to chemical engineering educators. Persons who wish to be placed on the mailing list should notify CACHE at the aforementioned address. Contributions from CACHE representatives are welcome. This issue was edited by D.M. Himmelblau with contributions from a number of CACHE members and representatives.

CACHE TASK FORCES AND COMMITTEES

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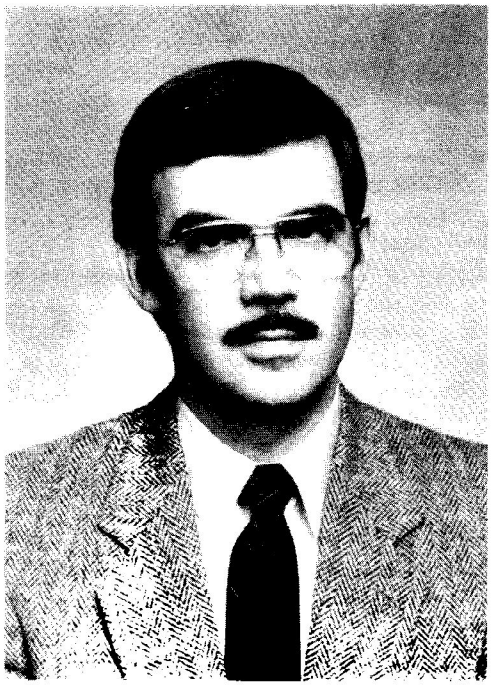

Prof. G.V. Reklaitis
President of CACHE

Professor Reklaitis is a professor of ChE and Asst. Dean Engr., Grad. Education & Research at Purdue University. He has been a CACHE Trustee since 1979 and previously was Secretary and later on Vice-President. His research interests are in computer aided process engineering and especially focussed on problems in batch processing. Teaching activities include undergraduate courses in Material & Energy Balances and Process Design; a dual level course in Engineering Optimization and graduate courses in Computer Aided Design and Applied Math. The Balances and Optimization courses both have led to Wiley textbooks.

His current educational project is focused on a Simulated Laboratory Experiments Project, a cooperative activity with sponsoring companies to produce a series of modules each consisting of an interactive simulation of a novel industrial operation, video tapes describing these operations and student materials describing objectives and background material of experiments to be conducted using the simulations. This project is being carried out jointly with Prof. Bob Squires (Purdue University). A module developed from Amoco data is completed, a module with Dow is nearing completion and additional modules are in the planning stages.

H. Scott Fogler
Vice-President of CACHE

H. Scott Fogler is Vennema Professor and Chairman of Chemical Engineering at The University of Michigan. He has been a member of CACHE Corporation for 10 years. His CACHE and computer related projects include co-editor of the CACHE CHEMI modules of kinetics, and development of a 9 interactive simulation in reaction engineering for use on the IBM PC.

He has research interests in flow and reaction in porous media, colloid stability, and dissolution kinetics in micro-electronics fabrication. He is author of over 80 research publications in these areas. In addition, he is author of two books, the most recent '*The Elements of Chemical Reaction Engineering*', was published by Prentice-Hall in May 1986. For the past 19 years he has been a consultant for Chevron Oil Field Research Company.

In 1980, he was a first recipient of the newly instituted awards for Outstanding Research from the University of Michigan College of Engineering, and also in 1980, received the Chemical Engineer of the Year Award from the Detroit section of the American Institute of Chemical Engineers. In 1984, he was appointed Vennema Distinguished Professor of Chemical Engineering. He is a Fall 1985 graduate of the New Orleans School of Cooking, is an avid Michigan baseball fan.

CACHE REPRESENTATIVES' RECEPTION MIAMI AICHE MEETING

The Annual Reception and Program for the CACHE Representatives and their guests will be held from 5:30 to 7:30 p.m. on Wednesday, November 5, 1986, in the East ballroom of the Fontainebleau Hilton.

We will feature three activities of CACHE:

1. Curriculum task force (Warren Seider). Posters describing the lessons plus a five-to six-minute talk highlighting what is available, plans for distribution, etc.

2. Artificial intelligence (George Stephanopoulos). Possible poster, plus five-to six-minute talk about the direction this task force is headed. This presentation is intended to show some of the new fields CACHE is entering, as background information. CACHE products are not expected.

3. Large scale task force (Bob Seader). Posterboard display of both SPEEDUP and FLOWTRAN optimization. In addition, a short presentation of thanks to Roger Sargent and John Perkins. Not a Technical presentation but simply a thank you.

Foundations of Computer-Aided Process Operations
July 5-10, 1987
Park City, Utah

The objective of this one-week specialist conference is to provide an in depth review of the state-of-the-art, general problems and research needs in the area of computer aided plant operations. The structure of the conference will parallel that of the CPC (Control) and FOCAPD (Design) conferences. Specifically, it will involve a limited number invited speakers and commentators, ample periods for discussion by the participants, a single contributed paper session organized in a poster session format, and a restricted number of attendees.

Program

The program of the meeting is nearly finalized and consists of the following sessions, speakers, and commentators:

Process Data Acquisition & Interfaces

John Hale, DuPont, chairman
Lawrence DeHeer, Engineering Department, DuPont
Plant Scale Process Monitoring and Control Systems
Prof. Richard Mah, Northwestern University
Data Screening
Dr. Patrick Kennedy, Oil Systems, Inc., Commentator

Process Safety

Prof. Gary Powers, CMU, chairman
Malcolm Preston, ICI, co-chairman
H.A. Duxbury and M.L. Preston, ICI PLC
Systems Engineering Issues in Process Safety
William Brasie, Dow Chemical
Human Factors in Process Operation Safety Analysis: The Computer/Human Interface
Prof. Gary Powers, Carnegie Mellon University
Probabilistic Risk Assessment
Prof. P. Andow, Loughborough University of Technology (UK), Commentator

Operations Planning

Prof. David Rippin, E.T.H., Zurich, chairman
Tony Perris, Air Products (UK) co-chairman
Charles White, DuPont
Application of OR methodology to Process Operations
B.A. Sigrist, Nestle SA, Vevey, Switzerland
Supply Chain Management in the Packaged Food Industry
Commentator to be confirmed

Maintenance Planning

Tony Perris, Air Products (UK), chairman
Prof. David Rippin, E.T.H., co-chairman
C.F.H. Van Rijn, MSE Dept., Shell Research, Amsterdam
A Systems Engineering Approach to Reliability, Availability, and Maintenance
Terry W. Williams, Stearns Catalytic Corp.
Systems Approach to Maintenance Planning
Frank Pierce, Union Carbide, Commentator

Process Simulation

Rufus Baxley, Union Carbide, chairman
J.D. Perkins, G.W. Barton, and R.M. Pitblado, University of Sidney
Modeling and Simulation in Process Operations
Toshi Shinohara, C.E. Simcon
A Block Structured Approach to Dynamic Process Simulation
R.F. Preston and G.B. Gochenour, Shell Oil Company, Houston
Equation Based Process Simulation
Prof. Jack Ponton, University of Edinburgh (UK), Commentator
Edward M. Rosen, Monsanto Co., Commentator

Process Optimization

Prof. Ignacio Grossmann, Carnegie Mellon University, chairman
John Tomlin, Ketron Inc.
Large Scale Mathematical Programming Systems for Process Operations
Prof. Arthur Westerberg, Carnegie Mellon University
Optimal Redesign and Modification of Existing Plants
David R. Heltne, Shell Development Co., Commentator
Jerry L. Robertson, Exxon R&D, Commentator

Plant Network and Databases

Norm Rawson, IBM, chairman
John Heafner, National Bureau of Standards
Plant Information Networks
Wil Plouffe, IBM Research
Manufacturing Databases in Distributed Environments

Charles H. Reese, Chevron Corporation
Plant Data Management: Practice and Futures
Prof. D. Grant Fisher, University of Alberta, Commentator

Intelligent Systems in Process Operations
Prof. George Stephanopoulos, MIT, chairman
Prof. George Stephanopoulos, MIT
The Scope of Artificial Intelligence in Plant-Wide Operations
Prof. Mark Kramer, MIT
Expert Systems for Process Fault Diagnosis: A General Framework
Profs. D.E. Lamb, D. Chester, P. Dhurjati, University of Delaware
Evaluation of Experience with an Expert System for Fault Diagnosis in a Commercial Scale Chemical Process
Brian Mathews, Exxon Chemicals, Commentator

Poster Session: Innovative Research in Process Operations
Prof. J. Douglas, University of Massachussetts, Amherst, chairman Rapporteur to be confirmed

The poster session, consisting of a limited number of contributed papers, will be held on Thursday afternoon (July 9). Authors interested in contributing a paper to this session should submit a title and two page abstract to the session organizer, Professor James Douglas, Dept. of Chemical Engineering, University of Massachusetts, Amherst, MA 01003 by January 1, 1987.

Conference Site

The conference will use the facilities of the Prospector Square Hotel which has both a fully equipped Conference Center an a complete Athletic Club. Accommodations include hotel rooms, studios as well as condominiums. Common breakfast and dinner services are planned at a cost. Park City, Utah, is a summer/winter mountain resort originally founded as a silver mining camp. The Park City area offers mountain hiking and horseback riding, tennis, golf, bicycling, ballooning and gliding as well as water sports at one of three reservoirs located within 25 minutes. As the largest resort community in Utah, Park City has interesting shops and boutiques, art galleries, and summer theater for the less athletically inclined. The town is 45 minutes by car from the Salt Lake City International Airport and is served by airport limos. The Salt Lake city area is within a few hours drive of famous national parks such as Yellowstone, Zion, Arches, the Grand Canyon and Lake Powell.

Application Form for Participants

Attendance at the FOCAPO Conference will be limited and is by invitation following receipt of an application form. Requests for application forms should be directed at the **CACHE office.** The deadline for the submission of applications is **January 15, 1987.** Selection of attendees will be made on the basis of involvement and experience in the field of computer aided process operations. Notifications of selection will be issued by March 15, 1987.

For further information about the technical program inquiries should be directed at the Conference Chairs:

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ANNOUNCING FOCAPD-PSE'89 CONFERENCE

Dr. Jeffrey J. Siirola of Tennessee Eastman has been designated the Conference Chairman, and Professor Ignacio Grossmann of Carnegie-Mellon University has been designated the Conference Co-Chairman for the next Foundations of Computer-Aided Process Design - Process Systems Engineering (FOCAPD -PSE'89) Conference. The Conference is jointly sponsored by CACHE and the CAST Division of AIChE. The date and location will be announced at a later date.

CACHE COMPUTER NETWORKING STUDENT CONTEST
CACHE Electronic Mail Task Force

BACKGROUND:

Computer networking has not yet made much of an impact on the chemical engineering community, a situation that probably exists in other engineering disciplines such as mechanical engineering, aerospace engineering, and civil engineering. Notwithstanding the CACHE National Electronic Mail experiment, if there were strong interest in this area, many more of our colleagues would already be using the "free" BITNET wide area network, which links hundreds of academic institutions in the United States and abroad.

At the moment, a critical mass of chemical engineering users of computer networking sometimes called electronic mail, does not exist. Faculty members are overcommitted and probably begrudge the time necessary to acquire hardware as well as learn commands and protocols for unfamiliar software.

Late 1984, when the CACHE National Electronic Mail experiment was first proposed, John Seinfeld (Caltech) suggested that the task force find ways to involve students, the ITT Dialcom Compmail+service, which charges users at a rate of $15 per hour during peak time, did not seem to be the appropriate network for student-oriented projects, and none were proposed.

With the movement of Task Force focus to BITNET, the cost of which is shared among the member academic institutions (and often appears as "funny money" to departments), an opportunity exists for students to participate in a communications effort that will play an important role in their future careers.

The CACHE Electronic Mail Task Force is initiating a nine-month contest directed towards AIChE student chapters, which will compete for a top prize that will be as high as $500 if a sufficient number of chapters participate. The details of the contest are as follows.

OBJECTIVE:

To generate and execute a project that potentially has lasting value in the area of computer networking among chemical engineering departments and among chemical engineering professionals.

RULES:

1. Only AIChE student chapters, or their Canadian, Mexican, or European equivalents, are elegible for the competition.

2. The prize is called the CACHE Student Chapter Award.

3. The wide-area network that must be used is BITNET.

4. A competing student chapter must submit, by March 31, 1987, a report that documents their computer networking project during the 1986-87 academic year. The report should contain a title page, a list of student participants, a table of contents, a summary of poject activities that is no longer than ten single-spaced pages, and appendices as required. Five copies of the report should be submitted by the stated deadline to Dr. Peter Rony, Department of Chemical Engineering, Virginia Tech, Blacksburg, Virginia 24061.

5. The submitted report must contain at least one appendix, which provides a step-by-step tutorial (perhaps written in cookbook style) on the local university use of BITNET. In this tutorial, a student or faculty user must be taught how to acquire a userid, get on the computer operating system, send a file to a BITNET user at another university, receive and store a file from BITNET user, and so forth. A good demonstration file or message is a BASIC or FORTRAN program that can be tested by the receiver.

6. Selected chemical engineering faculty will serve as consultants on BITNET for the student chapter competition. Their names and userids will be sent to competing student chapters late in October 1986.

7. If your student chapter wishes to compete, please send your local userids to Peter R. Rony at Virginia Tech within three weeks after the publication of the fall issue of *CACHE NEWS*. You will be placed on both postal and electronic mailing lists for further information.

8. The reports will be evaluated by a panel of at least three, and no more than five, chemical engineering educators who are active users of electronic mail. The chairman of this committee will be a member of the CACHE Board of Trustees. Peter Rony, Chairman of the CACHE Task Force on Electronic mail, will not be a member of the panel, but rather a consultant and monitor of the student competition.

9. The student project can start as soon as the announcement of the competition is received by the department. The competition will be announced both by mail and by an article in the fall issue of *CACHE NEWS*.

10. A student chapter can use university faculty and staff as BITNET consultants to reduce the time required to execute their project. The nature of the contributions of these consultants should be stated in the report. We appreciate the value of undergraduates' time, and would like them to use it as efficiently as possible.

11. The magnitude of the prize will depend upon the number of competing student chapters. No CACHE Student Chapter Award will be given if fewer than four chapters compete. For four or more competing chapters, the Award will be as follows:

4 to 8 chapters	$150 prize
9 to 15 chapters	$300 prize
More than 15 chapters	$500 prize

12. The initial testing of ideas on BITNET Acan be performed locally by a student chapter, which would use at least two local userids for such a purpose. A premium will be placed on communication among different student chapters on the BITNET network. Like the ham radio operator who keeps a list of station numbers as he communicates throughout the world, demonstration of success in the field will be one characteristic of the winning student project.

13. What type of contribution is of lating value? In a situation where computer networking is used rarely in chemical engineering, a lasting contribution would be one that creates a strong incentive for student and faculty colleagues to communiate via BITNET on a regular basis. Some projects that come to mind include:

- Creation and use of a special distribution list of chemical engineering students and educators who have a special interest of some type.
- Preparation for a regional student chapter meeting.
- Identification and dissemination of job opportunities for small businesses that wish to employ new chemical engineering graduates. Creation of a bulletin board of small businesses.
- Development and distribution of course materials.
- Involvement of a staff member at AIChE headquarters in New York City in the BITNET experiment. The student chapter would have to mount the campaign to convince AIChE to gain access to a BITNET node.
- Assistance in the conversion from paperwork to computer networking for selected aspects of the preparation for a national AIChE meeting.

• Assistance in the planning for a professional meeting involving chemical engineering educators.

• Cooperative activities among chapters that involve either research or education.

• Continuing education courses offered on a computer network, for example, one similar to the Continuing Education Computer-based Individualized Leanring Environment, or Cecile, created by Andrew Skey (SM), an associate research engineer at the University of California, Santa Barbara.

• Creation of a national listing of students (and brief biosketches) who are interested in attending graduate school starting the 1987-88 academic year.

These ideas only sample the possibilities of a poject of lasting value to the chemical engieering community. For recent comments on how computer networking is used by students in another engineering field, please see the end of the article, "Chemical Engineers Meet a Changing World," by J.F. Mathis *Chemical Engineering Progress,* 82 (7), 17-21 (July 1986). For further informtion about computer networking, consult the article, "Computer Networking for Scientists," in the February 28, 1986 issue of *Science.*

MICROCOMPUTER/PERSONAL COMPUTER NOTES

Peter Rony
Virginia Polytechnic institute & State University

Business Computer Systems (October 1985) briefly summarized progress on linguistics software, one of the faster growing niche markets in office automation (100 to 250 percent increase per year). Both ALPS and Weidner Communications Corp. have introduce IBM AT- and XT-based translations systems. Their cost is still high, $19,000 and $10,000, respectively, but is certain to decline significantly within five years. The same issue contains information on "Bridges and Gateways" between local area networks, high-quality graphics software, and three macro processors (Keyworks, SuperKey, and ProKey 4.0).

Byte's 10th Anniversary Issue (September 1985) had homebrewing as a theme. An article that caught your editor's eye, as a long-time 8080A/8085/Z80 microprocessor user, is "Build the SB180 Single-Board Computer," by Steve Ciarcia. The single-board 8-bit processor is based upon the Hitachi CMOS Z80-code-compatible processor, HD64180, which directly addresses 512 kbytes and has a number of important hardware goodies built into the 64-pin chip. The message that engineers should keep in mind is that the two major 8-bit family microprocessors (8080A and 6502) continue to thrive in tens of thousands of products that do not require 16-bit processors. By the end of the decade, a gallium arsenide Z80-family microcomputer should become commercially available that has a clock speed in excess of several hundred megahertz.

The September 1985 issue of *Byte* also contains "A Microcomputer Timeline" that summarizes key dates in the history of microcomputers starting with 1974. Not widely appreciated these days is the modest role that a small university town in Virginia--Blacksburg--played in the early days of homebrew microcomputer systems and microcomputer education. Included in the timeline is the July 1974 issue of *Radio-Electronics,* "Build the Mark-8, Your Personal Computer," developed by a Blacksburg chemistry graduate student, Jon Titus. Jon also developed the first microcomputer trainer, the MD-1, which was introduced in the summer of 1975 and incorporated solderless breadboarding techniques. The first university-originated textbook on microcomputers was published in Blacksburg in August 1975.

Need to construct a parallel-to-serial printer port adapter for your laboratory computer? See the article by Howard Austerlitz in the September 1985 issue of *Byte,* pages 257-260. Mark Hanslip shows you how to "Add Function Keys to Your Microcomputer," pages 263-268.

The October 1985 *Computer,* a publication of the IEEE Computer Society, is a special issue on computer-based multimedia communications. Articles focus on the electronic book, real-time conferencing systems, office document interchange formats, graphics standards, the DARPA multimedia mail systems, and a distributed interoffice mail system. "Computer Conferencing" is the subject of a series of nine articles in the December 1985 issue of *Byte* magazine.

"Telecommunications Standards Arrive" (pages 84-96 in the October 15 issue of *Datamation*) provides a provacative quote from J.A.N. Lee: "One quarter of the total available computer power in the U.S. is being used to provide conversion sytems between dissimilar, nonstandardized (or nonstandrd) elements of computer systems." The quote dates back to 1976, but apparently is valid today.

Dr. Dobb's Journal (September 1985) descrives "Two TEX Implementtions for the IBM PC" (Pages 80-91). TEX is a system for typesetting technical text developed by Donald Knuth. The October 1985 issue of *Dr. Dobb's* is dedicated to "The Future of Forth;" the characteristics of the Novix NC4000 processor, a threaded-code hardware microprocessor for the Forth language, are given. Specialized microprocessors designed for the execution of high-level languages--NC4000, Forth Engine, H. Forth, CLM, Spur, Soar, X-1, and ACAPS--are summarized in the February 6, 1986 issue of *Electronic Design* (pages 26-32.) *Electronics* magazine (November 25, 1985, pages 58-60) also treats this topic. Consider LISP-on-a-chip for AI applications in small computers and products that contain embedded microcomputers.

New computer jargon: silicon supermarket, which is defined as a chip fabrication company that can supply developers with all their computer-aided engineering needs under one roof.

Volume 10, Number 11 of *Byte,* a special IBM issue, contains several items of interest: (a) An editorial on Intel and

Future IBM PCs, the iAPX286/386, and the Motorala MC68000; (b) An annotated bibliography of recent books on the IBM PC family (pages 11-35); (c) Public-domain utilities for the IBM PC (pages 39-54); (d) A discussion of important differences between the 8088 and 80286 microprocessors (pages 93-101); (e) Programming suggestions on the writing of desk accessories (pages 105-122); (f) Benchmarks of IBM PC clones (pages 195-201); and (g) IBM PC-family BIOS comparisons (pages 259-265).

Digital signal processors will be the subject of a presentation at the Annual AIChE Meeting in Miami Beach; new DSP chips are described in the August 26, 1985 issue of *Electronics* (pages 42-46).

Electronics (formerly *Electronics Week*) is recovering from its brief excursion into magazine mediocrity. Items of interest include a 68020-based microcomputer that runs IBM 370 mainframe software (August 19, 1985, page 47).

The November 1985 issue of *Byte* magazine provides extensive hardware and software (BASIC) details about the XECOM XE1203 MOSART module, "The World's Smallest 1200-bps Modem" (pages 89-108). In the same issue, Mark Bridger and Mark Goresky show you how to produce "High-Resolution Printer Graphics" (pages 219-232) by addressing the individual dots used to generate printed dot-matrix characters.

Ralph Levien, in the February 1986 issue of *Byte*, describes a LISP editor that lets you relate LISP programs visually ("Visual Programming," pages 135-144). Golden Common LISP, a variant of Common LISP, which is "a standard LISP blessed by the Department of Defense) is reviewed in the December 1985 *Byte* (pages 317-321). Grapes is the name for Advanced Computer Tutoring's AI-based system for learning LISP *Electronic Design*, November 28, 1985, page 38).

Ten programming editors/programmable editors for MS-DOS are compared from the standpoint of features, size, documentation and help, editing commands, search and replace, file and window management, text formatting commands, printing, undo, keystroke macros, macro language, subprocesses, error handling, benchmarks, miscellaneous features, and overall evaluation in the November 1985 issue of *Dr. Dobb's Journal*. The difference beween Modula-2 and Pascal for microcomputers is also discussed.

An elegant way to bring up a 68000 microcomputer as a free-running system is described by Alan D. Wilcox in the January 1986 issue of *Dr. Dobb's Journal* (pages 60-74). Excellent block diagrams, schematics, and timing diagrams are provided. The article may be useful for those hardy souls who are working with 68000-based laboratory computer systems.

Have you ever wondered what a cyclic redundancy check (CRC) does in detecting errors in data transmission? If so, you should read "The Great CRC Mystery," by Terry Ritter in the February 1986 issue of *Dr. Dobb's* (pages 26-34).

Project-management software is the focus of a product report in the December 12, 1985 issue of *Electronic Design* (pages 149-158). Forty-two products are included in the published directory.

A glimpse at future developments in microelectronics technology can be obtained by studying the 1986 Technology Forecast published in the January 9, 1986 issue of *Electronic Design*. The 50 to 200 chips on a single printed circuit board will be consolidated, in several years, into several large VLSI integrated circuits. Some of the articles are on software tools for IC design, electronic breadboarding, analog standard cells, programmable logic devices, and a silicon complier tool set.

The feature article in the January 23, 1986 issue of *Electronic Design* (pages 73-82) is the Texas Instruments TMS34010 32-bit CMOS graphics processor. It uses a 6 million instructions per second (6 MIPS) general-purpose instruction set and special pixel-processing instructions and handles bit-mapped graphics.

The one-chip modem is described in the November 5, 1985 issue of *Electronics* (pages 46-52), making it easier to build modems into a variety of products that require serial communications.

For $95, you can purchase "Pocket APL," an inexpensive yet complete version of the language for an IBM PC. Details and benchmarks are given in the March 1986 issue of *Byte* (pages 237-243). "68000 Wars: Round 1" between the Macintosh, Amiga, and Atari 520ST are discussed by Bruce Webster in the same issue (pages 305-322).

Do ASCII-based communications have a future relative to more advanced protocols such as IBM's Systems Network Architecture (SNA) protocols? The question is discussed by Michael Tucker in the November 1985 issue of *Mini-Micro Systems* (pages 119-124).

Curious how a windowing environment manages memory? *PC Magazine* treats GEM Desktop, Microsoft Windows, TopView, and DESQview in the February 25, 1986 issue (pages 108-132). I vowed not to worry about word processors anymore in this column, but must mention the extensive discussion of new products by John Dickinson in the same issue (pages 177-214).

"CAD: The Big Picture for Micros," is the cover of the March 11, 1986 issue of *PC Magazine* (pages 108-180). A major series of article. "The IBM Token-Ring LAN: What? Why? Now?" appeas in the same issue. In the March 25, 1986 issue of the same magazine, the IBM Enhanced Graphics Adapter (CGA) standard and color monitors are featured (pages 108-144).

A hint at the future: parallel-processing engines *Electronics*, November 18, 1985, pages 23-24). Two companies are preparing hardware that will turn an IBM PC AT into a multiple-

processor parallel engine. ITT's massively parallel Personal Supercomputer Coprocessor, slated for a 1987 debut, is expected to handle 120 million 32-bit floating-point operations per second and provide 100 Mb/s of external I/O bandwidth.

Read about "Optical ICs: The New Alternative" in the November 18, 1985 issue of *Electronics* (pages 39-44). The bulk of R and D has focused on integrating optical components, constructing optoelectronic components that combine electronic and optical logic elements onto the same monolithic substrate, and fabricating vertical superlattice structures.

In the "Battle of the Buses: And the Winner Is ..." *Electronics*, November 25, 1985, pages 48-51), the Motorola/Mostek/-Signetics 32-bit VME hardware bus has a three-year head start over the Intel 32-bit Multibus II. For 8- and 16-bit systems, Intel's Multibus I has been dominant.

The December 23, 1985 issue of *Electronics* has several stories on VLSI analog chips, which are following in the footsteps of digital VLSI, and "The Big News at ISSCC: Digital Signal Processors." An article by Bernard Conrad Cole (pages 50-52) summarizes developments in analog technology, signal processors, general-purpose processors, semicustom ICs and arrays, and memories presented at the International Solid-State Circuits Conference in February 1986. IBM has a 32-bit single-chip microprocessor that incorporates 102 mainframe instructions and supports emulation of the rest of the instruction set. The followup article in the February 17, 1986 issue of *Electronics* (pages 23-31) describes these developments in greater detail. More on ISSCC--digital chips, analog chips, and special-purpose chips--is contained in the February 20, 1986 issue of *Electronic Design.*

A "smart analog IC" is a semiconductor circuit in which the analog and digital worlds have been merged. Analog operations occur under the watchful control of digital logic. See *Electronics,* January 20, 1986, pages 21-22.

"Slamming the Door on Data Thieves" *Electronics,* February 3, 1986, pages 27-31) presents some tutorial information on different forms of data encryption, including cipher-block chaining, cipher feedback, and output feedback.

STATUS OF FLOWTRAN LOAD MODULES FOR UNIVERSITY COMPUTERS

As part of a continuing program of support to educatin, Monsanto Company announced on August 19, 1982, that load modules for the FLOWTRAN simulation program would be made available on magnetic tape or other media to departments of chemical engineering to install on their own in-house computers. Thus departments would be able to run FLOWTRAN on their own computers at no charge other than that of their own computer center. CACHE is continuing the supervision of the preparation of FLOWTRAN load modules for a wide variety of mainframe, supermini, and supermicro-type digital computers and the distribution of the modules on magnetic tape or other media to those departments that order them. Instructional books on FLOWTRAN are already available through CACHE by using the order form at the end of this newsletter. FLOWTRAN is now available for the following computers:

1. **DEC VAX 11-7XX** series of super minicomputers running with the VMS operating system.
2. **DEC 20XX** mainframe computer running with the FORTRAN-20, Version 7 compiler (9-track, 1600 BPI tape).
3. *UNIVAC 1100* series computers running under the EXEC 1100 (38R2/08) operating system with the FORTRAN 77-SID (10R/A) compiler (9-track, 1600 BPI tape).
4. **Amdahl** computers running under the MTS (Michigan Terminal System) operating system with a FORTRAN Level G or H compiler (9-track, 6250 BPI tape).
5. **IBM** and IBM-Plug—Compatible mainframe computers such as the 370, 30XX, and 43XX with the following operating system and FORTRAN compiler combinations:

Version	Operating System	FORTRAN Compiler
a	VM/CMS	VS
b	OS1/MVS	IV-H est
c	OS/VS2 MVS	VS
d	MS	IV-G1

6. **IBM PC-XT-370** personal computer operating in conjunction with an IBM mainframe.
7. **CDC Cyber** mainframe computers with the NOS operating system and a FORTRAN V compiler.
8. **Apollo Domain** with stations running with AEGIS operating system (program on floppy disks).
10. **DEC MicroVAX II** with the VMS operating system.

Conversions are also underway for the DEC 10, Honeywell, Sperry 90/80, DEC VAX under UNIX, and Prime machines. Each FLOWTRAN tape contains either load and/or relocatable code, test problems and solutions, and installation instructions. The FLOWTRAN program may be used for educational purposes but not for consulting. A total of 135 FLOWTRAN tapes and floppy disks have already been distributed. The following universities have received FLOWTRAN during 1986:

University	Computer	Operating System
The Univ. of Alabama in Huntsville	UNIVAC 1100	EXEC
California State Poly. University, Pomona	DEC VAX 11-750	VMS
Carnegie-Mellon University	HP200	UNIX
Inst. Tec. de Celaya	DEC MicroVAX II	VMS
Katholieke Universiteit Leuven	Amdahl 470/V8	VM/CMS

Lafayette C.	DEC VAX 11-750	VMS
University of Maine	IBM 3033, 4381	VM/CMS
University of Maribor	DEC VAX 11-750	VMS
University of Massachusetts	CYBER 830	NOS
University of Michigan	Apollo DOMAIN	AEGIS
University of Minnesota	Apollo DOMAIN	AEGIS
University of Nevada at Reno	DEC PDP 11-73	UNIX 5.2
(Brooklyn) Poly. Inst. New York	DEC MicroVAX II	VMS
Univ. of Rhode Island	DEC VAX 11-780	VMS
The University of Texas	DEC VAX 11-780	VMS
Univ. Tecn. Federico Santa Maria	DEC 2020	TOPS 10
Universidad de la Republica	IBM 4341	VM/CMS
Universidade de Coimbra	DG MV/8000	AOS/VS
University of Utah	DEC MicroVAX II	VMS
University of Utah	IBM 4381	VM/CMS

If you would like to obtain a FLOWTRAN tape for your computer and have not already expressed the desire to CACHE, complete and submit the form, FLOWTRAN TAPE, at the end of this newsletter. You will be required to sign a User's Agreement that must be approved by Monsanto. The cost of the tape, payable to CACHE, is $250. However, the charge to CACHE-supporting departments, listed near the end of this newsletter, is only $175.

EQS CHEMICAL EQUILIBRIUM AND STOICHIOMETRY ALGORITHMS

The EQS software package computes chemical equilibria in complex chemical systems consisting of up to 50 copies and 10 elements on an IBM PC or true compatible microcomputer. The software will also compute sets of stoichiometric reactions for chemical systems composed of up to 53 species and 11 elements. The programs are ideal for student or classroom use in conjunction with the topics of stoichiometry and/or multi-reaction equilibria in a thermodynamics course, as well as for research purposes.

The standard type of equilibrium problem treated is a single ideal phase (gaseous, liquid, or solid). However, certain multiphase problems can also be handled. The user may specify either fixed (T,P) or fixed (T,V), as well as Henry's or Raoult's law ideality in a liquid phase. A number of special types of problems and restricted equilibria such as fixed-pH problems in aqueous solutions.

User input is fully interactive, and input data files may be stored on disk for later use. Output may be sent to a printer and/or a disk file. The input data required for an equilibrium calculation consist of a list of the species and their chemical formulae, free energy data (equilibrium constant data for reactions or species free energies of formation), either (T,P) or (T,V) as appropriate, and the starting system composition.

The algorithms incorporate recent advances in this area, and have been recently developed by W.R. Smith, co-author with R.W. Missen of *"Chemical Reaction Equilibrium Analysis: Theory and Algorithms"*, Wiley-Interscience, 1982. Equilibrium calculations for a typical 22 species, 4 element system (equivalent to 18 reactions) take only 20 seconds on a standard PC (no 8087 co-processor is required), with smaller systems taking correspondingly less execution time.

The software is available from:

Separatrix Data Systems
36 Columbus Crescent
Guelph, Ontario
CANADA N1G 3A7

Cost is $200 plus $10 shipping/handling.

MICRO- and PERSONAL COMPUTER APPLICATIONS IN THE LABORATORY

One hundred fifteen replies to the CACHE questionnaire on undergraduate experiments involving on-line computer applications have been received. This large response has encouraged CACHE to prepare two documents for publication and distribution.

The first publication will summarize the information provided in the replies to the questionnaire. It will include a list of schools that have responded to the questionnaire along with the names of the respondents, the titles of all the experiments available and under development, and a list of computers and computer interfaces used. The document will also give, for each experiment, a list of schools with that particular experiment operational and a list of schools that are developing it. This summary of the questionnaire will represent an accurate and concise catalog of laboratory experiments involving on-line computers that are available within chemcial engineering departments at the present time.

The second publication is intended to be an anthology of selected experiments. Detailed information (6 to 8 pages in length) about each experiment will be provided. This document will contain a bibliography on undergraduate experiments with on-line computer applications and a section on various alternatives in configuring on-line computer systems, hardware and software ideas, etc. It should serve as a valuable resource for people wishing to develop similar facilities during the next half dozen years, since the emphasis will be on the experimental facility and its educational utility, not on the computer alone which might quickly become dated.

Concerning the summary of questionnaire responses, publication this fall is anticipated. As for the anthology of selected experiments, persons interested in participating in this project presently are being identified. If you would be interested in participating in this project we ask that you submit a one-page abstract describing each experiment that

you or your colleagues would like to have considered for inclusion. Only experiments that have been class tested will be accepted. When the final selection is made, the format for preparation of the 6-8 page summaries will be provided. Also, we would be interested in receiving a reprint of any papers you may have published on undergraduate experiments with on-line computer applications along with a full bibliographical reference. This material would enable us to compile the bibliography mentioned above.

The production of these documents will represent a major dissemination of information in the important area of laboratory applications of computers. It also will be the first opportunity to update on-line computing applications methodology since the CACHE Monograph Series in Real-Time Computing was published more than a half dozen years ago.

If you are interested obtaining further information or in participating in development of the anthology, please contact either:

Professor Ali Cinar
Department of Chemical Engineering
Illinois Institute of Technology
Chicago, IL 60616

or

Professor Duncan Mellichamp
Dept. of Chemical and Nuclear Engineering
University of California
Santa Barbara, CA 93106

COMPUTING TECHNOLOGY IN COURSES OTHER THAN DESIGN AND CONTROL

The CACHE Curriculum Task Force has been working to facilitate the use of computing technology in the core chemical engineering courses, where computer use has traditionally been inadequate, through the development and distribution of microcomputer-based lessons. These lessons are expected to utilize the computer in order to give students an opportunity to deal with open-ended (i.e., "design") problems at all stages of the curriculum, and not just in the capstone Process Design course.

At this writing, seven lessons are in various stages of development and testing. The following four are expected to be released later this Fall:

(1) *Design of a Gas-liquid Scrubber,* by D. Huang and J.H. Seinfeld, Cal. Tech., for the Separations Course. The analysis involves integration of the mass and energy balances, involving chemical equilibrium for absorption of SO_2 in the liquid droplet phase.

(2) *Heterogeneous Reaction Kinetics,* by H. Scott Fogler, Michigan. This lesson involves the selection of an appropriate rate expression to match the experimental observations.

(3) *Dehydration of Ethanol by Supercritical Extraction,* by J. Kellow, M. Cygnarowicz, and W.D. Seider, Penn. This lesson involves the comparison of designs for supercritical extraction using CO_2 with azeotropic distillation.

(4) *Flash Separation Compared with Distillation,* by Bruce A. Finlayson, Univ. of Washington. This program enables the student to adjust the design specifications and compare the costs of flash and distillation separations. It is well-suited for use in the thermodynamics and separations courses.

These lessons will be demonstrated at the CACHE Reception on Wednesday evening at the Miami Meeting of AIChE. Plans for their distribution on diskettes will also be announced.

Others are encouraged to participate in this project. Monies are available to help faculty obtain student assistance in the preparation of these programs. If you are interested, please contact Profs. Warren D. Seider or Morton M. Denn.

W.D. Seider
M.M. Denn

LIST OF CHEMICAL ENGINEERING DEPARTMENTS SUPPORTING CACHE

Last fall, CACHE solicited universities for funds to carry out on-going CACHE activities and to provide seed money for new projects. Departments providing support for the 1985-87 period, as well as for the 1984-86 period, are as follows:

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University of Virginia
University of Washington, Seattle
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West Virginia University
University of Wisconsin-Madison
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University of British Columbia
University of California, Berkeley
Clemson University
Colorado School of Mines
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Ecole Polytechnique-University of Montreal
Georgia Institute of Technology
University of Houston
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Send the form to:

Professor J.D. Seader
CACHE
3062 MEB
University of Utah
Salt Lake City, UT 84112

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CACHE Process Design Case Study Vol. 2
DESIGN OF AN AMMONIA SYNTHESIS PLANT

Preliminary Design and Economic Analysis

Summary: The objective of the case study is the design of an ammonia synthesis plant that is to be built in 1990, and that uses hydrogen and nitrogen feedstocks from a coal gasification plant. All stages of the design procedure starting from preliminary calculations down to the detailed flowsheet calculations are described. Emphasis is placed on the following steps: screening of key flowsheet decisions (pressure of synthesis loop, ammonia recovery, synthesis of gas recycle, hydrogen recovery from purge stream), selection of reactor configuration, cost minimization, and synthesis of heat exchanger network.

The proposed design incorporates a medium-pressure synthesis loop with water absorption/distillation for ammonia recovery, and with membrane separation for hydrogen recovery. The process was designed with the simulator PROCESS from Simulation Sciences, and the ammonia reactor was designed with the special purpose package QBED. A listing of this program is included in the case study. Depending on the required detail and the availability of process simulation software, the case study is suitable as a one-term assignment for a single student or a group of students. The preliminary calculations of the case study were performed by a group of three students, while the final design report is based on the work of a group of five students.

The problem statement was supplied by Philip A. Ruziska from Exxon Chemicals, and the case study was prepared under the supervision of Ignacio E. Grossmann from Carnegie-Mellon University.

CACHE Process Design Case Study Vol. 3
DESIGN OF AN ETHANOL DEHYDROGENATION PLANT

Preliminary Design and Economic Analysis

Summary: The objective of this case study is the preliminary design of an acetaldehyde synthesis process by ethanol dehydrogenation. The project covered all stages of the design procedure starting from consideration of qualitative aspects of the flowsheet and preliminary calculations to detailed process simulations and final economic evaluations. In this study emphasis is placed on synthesizing a workable flowsheet and justifying its configuration, simulating and evaluating the design using a commercial process simulator, and deriving a heat recovery network for the final process.

The main reaction in this process is the endothermic dehydrogenation of ethanol to acetaldehyde. However, under the specified reactor conditions, a number of byproducts are produced and their presence determines a number of interesting alternatives for separation. Once these alternatives have been screened and a workable flowsheet has been synthesized, the study centers on the simulation of this flowsheet using PROCESS from Simsci, Inc. Here, some of the features, advantages and limitations of this simulator are presented. Finally, the study concludes with a complementary presentation of this process simulated with the CACHE version of FLOWTRAN. While the aim of this study is not to provide a detailed comparison between PROCESS and FLOWTRAN, a useful description of the relative merits of both simulators can be readily observed.

This project is suitable for a one-term project by a five or six person team of senior design students. The results of two such teams are given in this study.

This problem was posed by the Union Carbide Corporation and the case study was prepared under the supervision of L.T. Biegler of Carnegie-Mellon University and R.R. Hughes of the University of Wisconsin.

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TOTAL _____

*Module requires that a copy of the MicroSoft FORTRAN-77 compiler be available.

These modules should be used only on PCs with hard disks (e.g., XT,AT).

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Foundations of Computer-Aided PROCESS DESIGN

Editors: **Arthur Westerberg**
Carnegie-Mellon Univ.

Henry H. Chien
Monsanto Company

This 1050 page hard-bound volume features 22 papers by leading academic and industrial researchers in the computer-aided design field. The major topics (**see backside for complete list of papers and authors**) are:

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4. Computational Algorithms
5. Physical Properties for Design
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Foundations of Computer-Aided Process Design

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